

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Kenichi TOKANO, et al.

SERIAL NO: NEW CONTINUATION-IN-PART APPLICATION

GAU:

FILED: HEREWITH

EXAMINER:

FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97**

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

**REFERENCES**

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**RELATED CASES**

- ☒ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**CERTIFICATION**

- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

**DEPOSIT ACCOUNT**

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters

Registration No. 28,870

Customer Number

**22850**

Tel. (703) 413-3000  
Fax. (703) 413-2220  
(OSMMN 05/03)

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**CERTIFICATION**

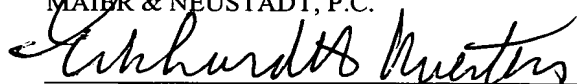
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Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. <b>250637US2S CIP</b>		SERIAL NO. <b>New CIP Application</b>	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT <b>Kenichi TOKANO, et al.</b>			
				FILING DATE <b>Herewith</b>		GROUP	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,040,600	03/21/2000	UENISHI ET AL			
	AB	4,754,310	06/28/1988	COE			
	AC	5,438,215	08/01/1995	TIHANYI			
	AD	6,410,958	06/25/2002	USUI ET AL			
<b>FOREIGN PATENT DOCUMENTS</b>							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES                      NO		
	AD	10-284591	10/23/1998	JAPAN			X
	AE	2000-208527	07/28/2000	JAPAN			X
	AF	9-266311	10/07/1997	JAPAN			X
	AG	2000-504879	04/18/2000	JAPAN			X
	AH	2000-260982	09/22/2000	JAPAN			X
	AI	8-222735	08/30/1996	JAPAN			X
	AJ	11-233759	08/27/1999	JAPAN			X
	AK	2000-183348	06/30/2000	JAPAN			X
	AL	7-7154	01/10/1995	JAPAN			X
	AM	2001-111050	04/20/2001	JAPAN			X
	AN	2000-323706	11/24/2000	JAPAN			X
	AO	7-176692	07/14/1995	JAPAN			X
	AP	8-64690	03/08/1996	JAPAN			X
	AQ	2001-298191	10/26/2001	JAPAN			X
	AR	0 587 176 A2	03/16/1994	EUROPEAN		X	
	AS	EP 0 732 749 A2	09/18/1996	EUROPEAN		X	
	AT	0 665 595 A1	02/08/1995	EUROPEAN		X	
	AU	WO 01/03202 A1	01/11/2001	WIPO (w/ENGLISH ABSTRACT)			X
	AV	DE 197 48 523 A1	05/12/1999	GERMAN			X
	AW						
<b>OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
	AW						
	AX						
	AY						
	AZ						<input type="checkbox"/> Additional References sheet(s) attached
Examiner					Date Considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

Docket No: **250637US2SCIP**

Serial No: **New Continuation-In-Part Application**

Filed: **Herewith**

For: **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING  
THE SAME**

STATEMENT OF RELEVANCY

**Japanese Application No. P2000359762. This reference proposes a structure and process for realizing a super junction structure used in a MOSFET of 400V or higher by deep trench, ion simultaneous implantation and separation of insulating layer.**

**Japanese Patent Application Laid Open No. 9-266311. This reference discloses a semiconductor device including a parallel drift path group having a plurality of first conductivity type divided drift path regions and second conductivity type partition regions adjacent thereto in which the first conductivity type divided drift regions have an oblong shape.**

**Japanese Patent Application Laid Open No. 2000-208527. This reference discloses a semiconductor element in which the p,n-regions of the super-junction elements are formed by ion implantation and heat diffusion. For both of p and n cases, impurities are introduced to an adjacent portion of the surface layer and a junction is formed in a middle by heat diffusion, to satisfy the relationship:  $y > x$  where  $x$  represents the width of the junction and  $y$  represents the depth (for both of p and n).**

**Japanese Patent Application Laid Open No. 10-284591. This reference discloses a method of manufacturing the semiconductor device, which has cells insulated and separated by a trench, wherein the trench is filled with an insulation layer and polysilicon layer, and a part of the polysilicon layer on the substrate is removed.**

**Japanese Patent Application Laid Open No. 8-222735. This reference discloses a planar gate MISFET that has a deep trench that reaches the substrate and a high-concentration N drain drift layer on its side walls, and the deep trench is filled with an oxide film. The drain drift region is an impurity diffusion layer, and it is formed by an oblique implantation and thermal diffusion (heat process) carried out on the inner surface of the trench.**

Docket No: 250637US2SCIP  
Serial No: New Continuation-In-Part Application  
Filed: Herewith  
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING  
THE SAME

Sheet 2 of 2

**Japanese Patent Application Laid Open No. 2000-260982. This reference discloses that the first conductivity type drift region is formed within a trench made in the first conductivity type semiconductor epitaxial layer on a semiconductor substrate, and a part of the base region is formed to have the second conductivity type in a stripe manner around the trench side wall to surround the drift region.**

**Japanese Patent Application Laid Open No. 2000-504879. This reference discloses that a depletion region and a complimentary depletion region, which have conductivity types different from each other, are put in a source-drain load zone of a semiconductor substrate, and the range of the concentration obtained by doping with the first conductivity type impurity is substantially the same as the range of the concentration obtained by doping with the first conductivity type impurity.**

**Japanese Patent Application Laid Open No. 7-7154. This reference discloses that there is repetitions of P layer / N layer in the N-layer, by which the layer is completely depleted. The P/N repetitions are made in parallel with the base-drain line.**

**Japanese Patent Application Laid Open No. 11-233759. This reference discloses that the first and second conductivity type sections in the voltage support region, and these sections have substantially the same size and should preferably have a columnar shape. These sections are of a vertical type, and the width of each section is smaller than its thickness.**

**LIST OF RELATED CASES**

<u>Docket Number</u>	<u>Serial or Patent Number</u>	<u>Filing or Issue Date</u>	<u>Inventor/ Applicant</u>
215568US2S	6,410,958	06/25/02	USUI et al.

EHK/akh

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